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(54) **ORGANIC LIGHT EMITTING DIODE DISPLAY AND MANUFACTURING METHOD THEREOF**

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(57) **ABSTRACT**

An OLED display according to an exemplary embodiment includes: a substrate; a gate insulation layer that is disposed on the substrate; and a gate wire that is disposed on the gate insulation layer, and includes a gate electrode, wherein the gate wire includes a single layer of aluminum or an aluminum alloy, and an angle formed by side surfaces of the gate wire and the gate insulation layer is less than 65°.

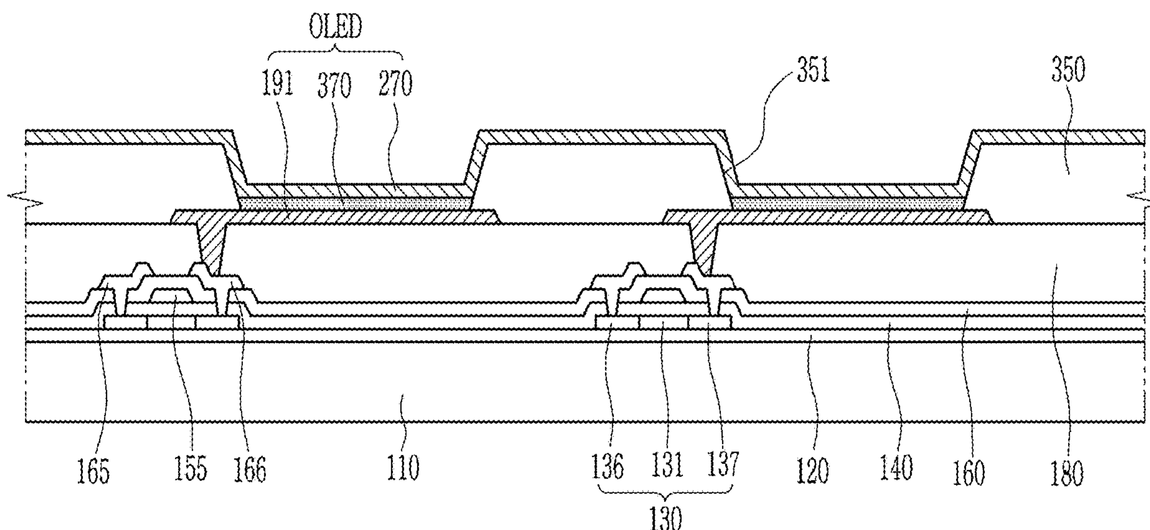


FIG. 1

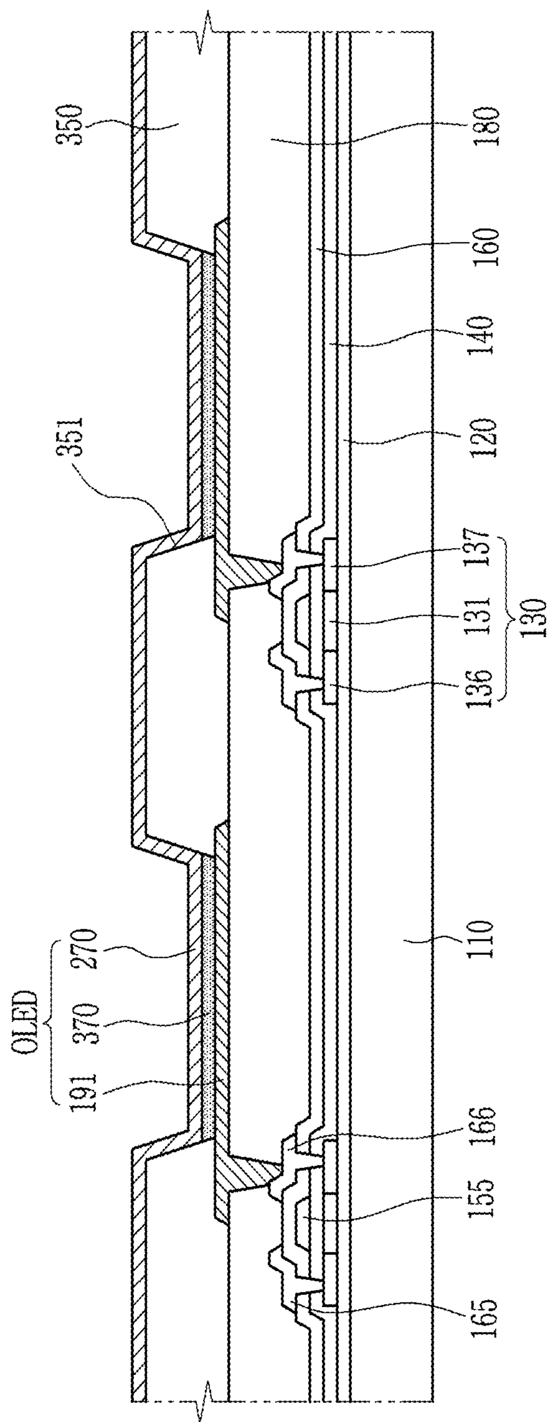
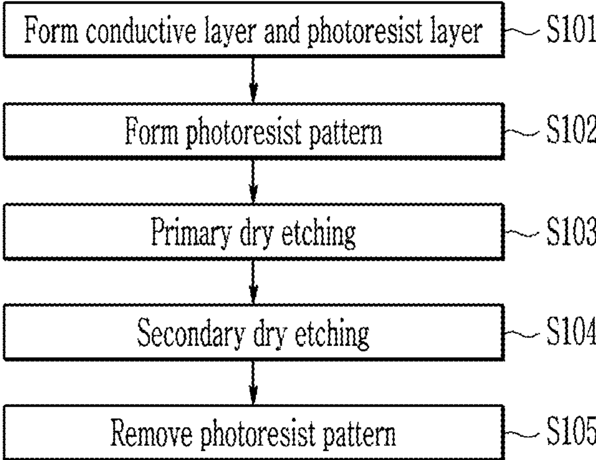


FIG. 2



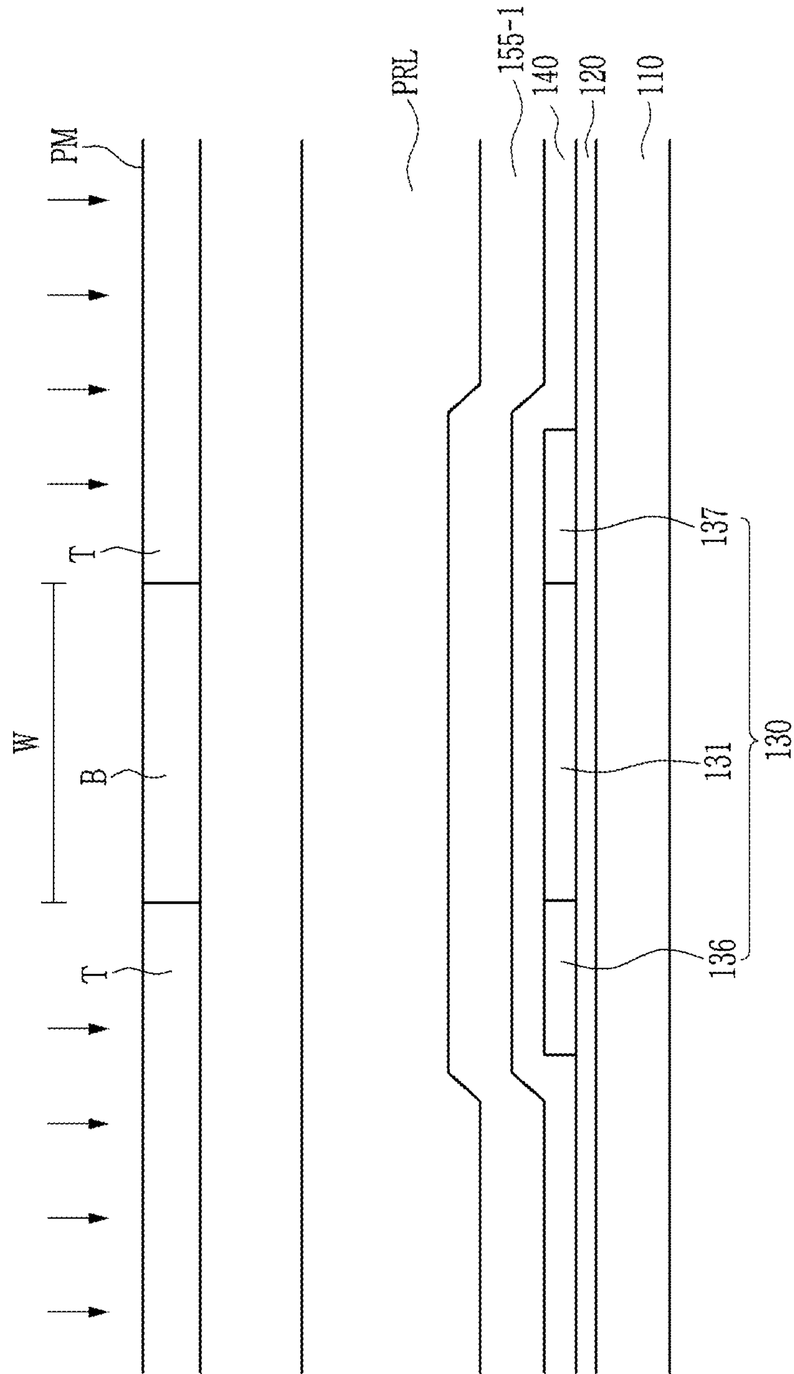


FIG. 3
PM
T
W
B
T
PRL
155-1
140
120
110
137
131
136
130

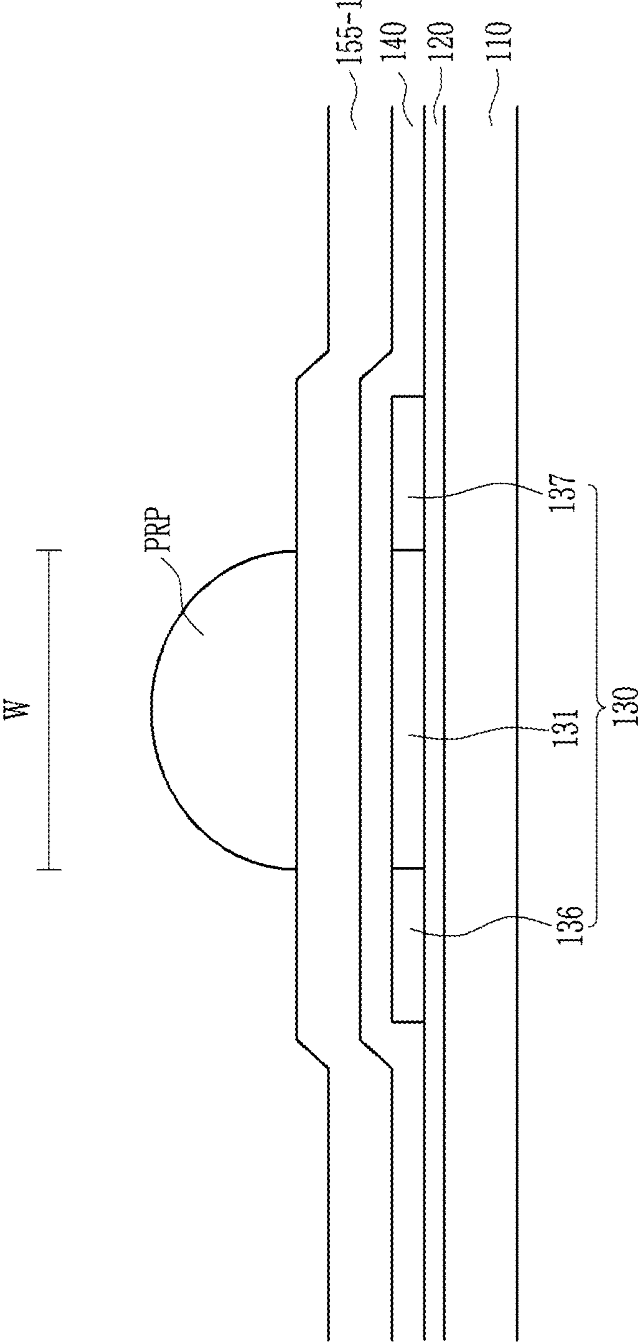


FIG. 4
W
PRP
155-1
140
120
110
137
131
136
130

FIG. 5

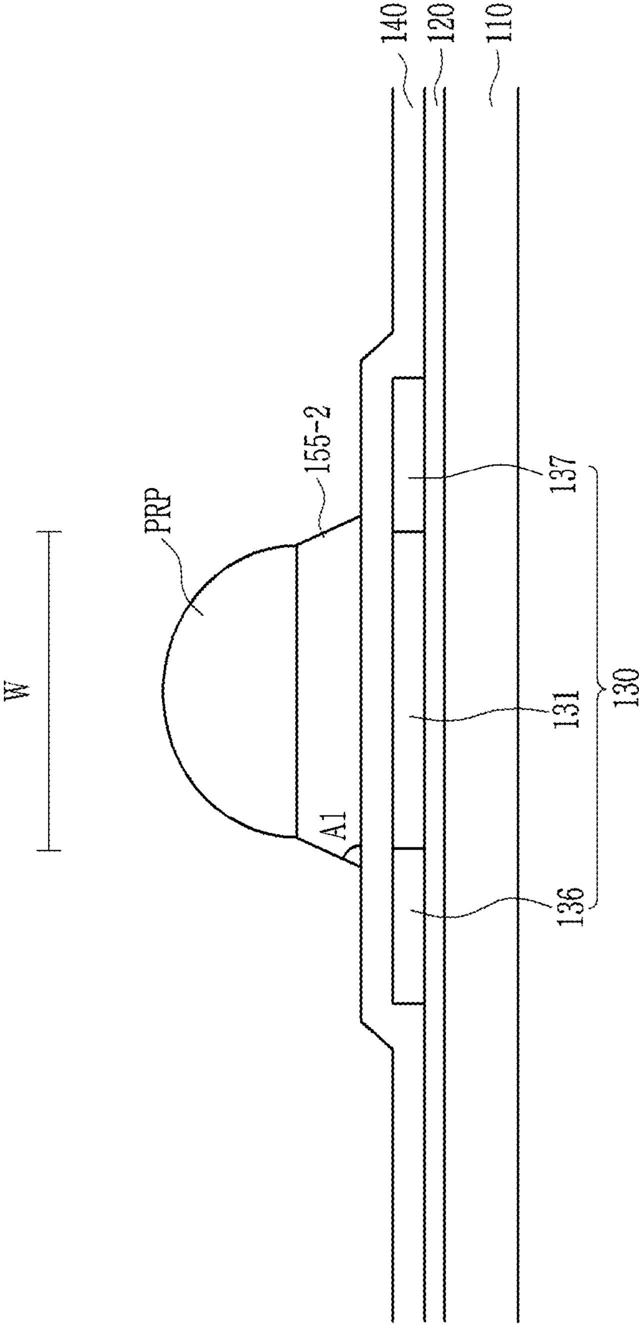


FIG. 6

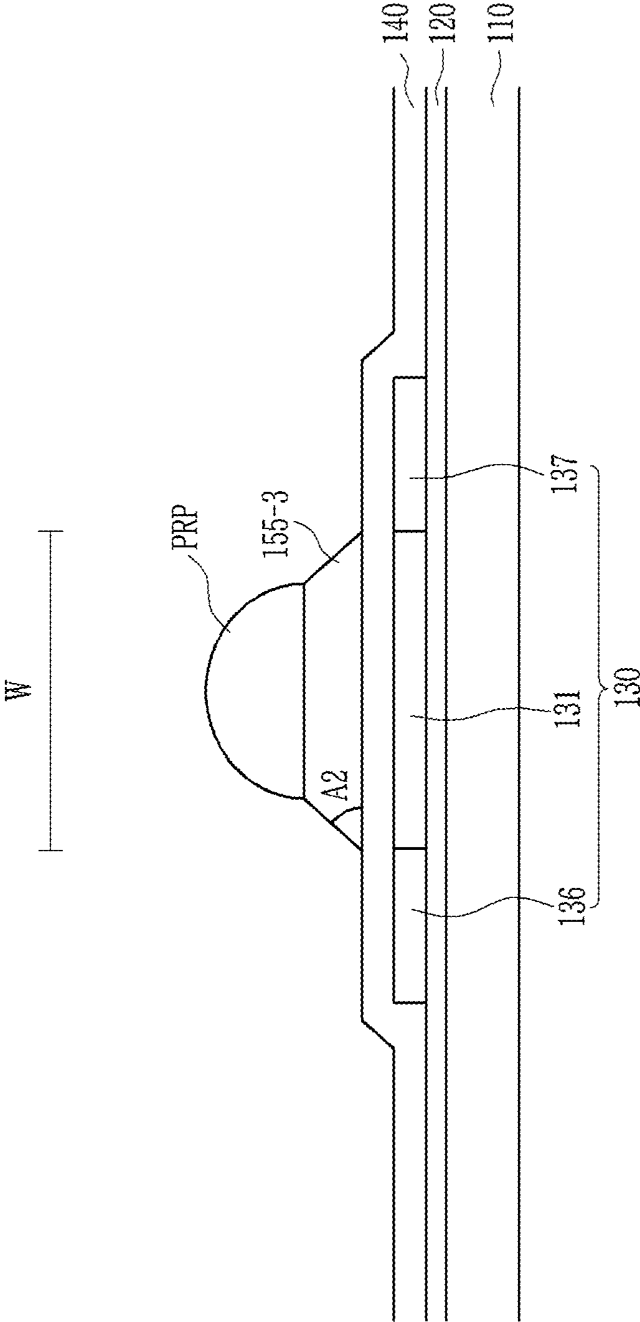


FIG. 7

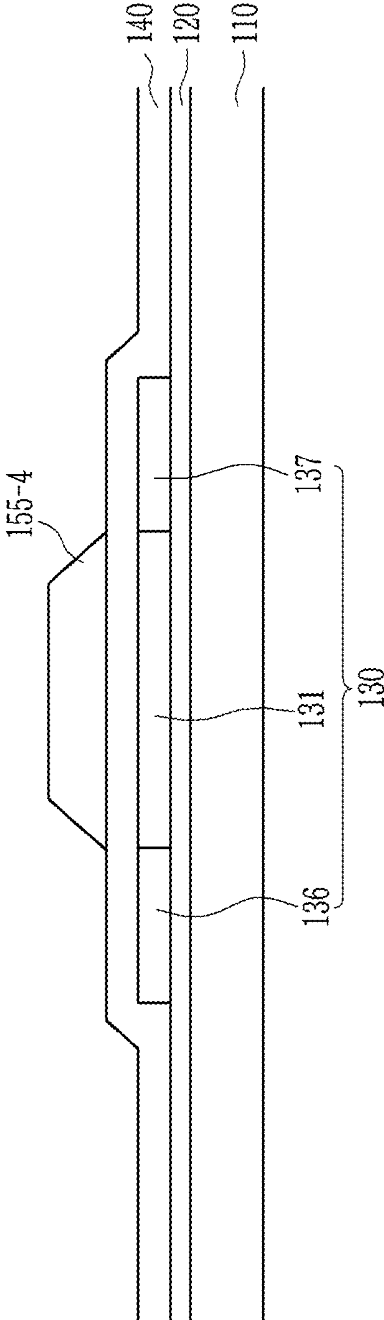


FIG. 8

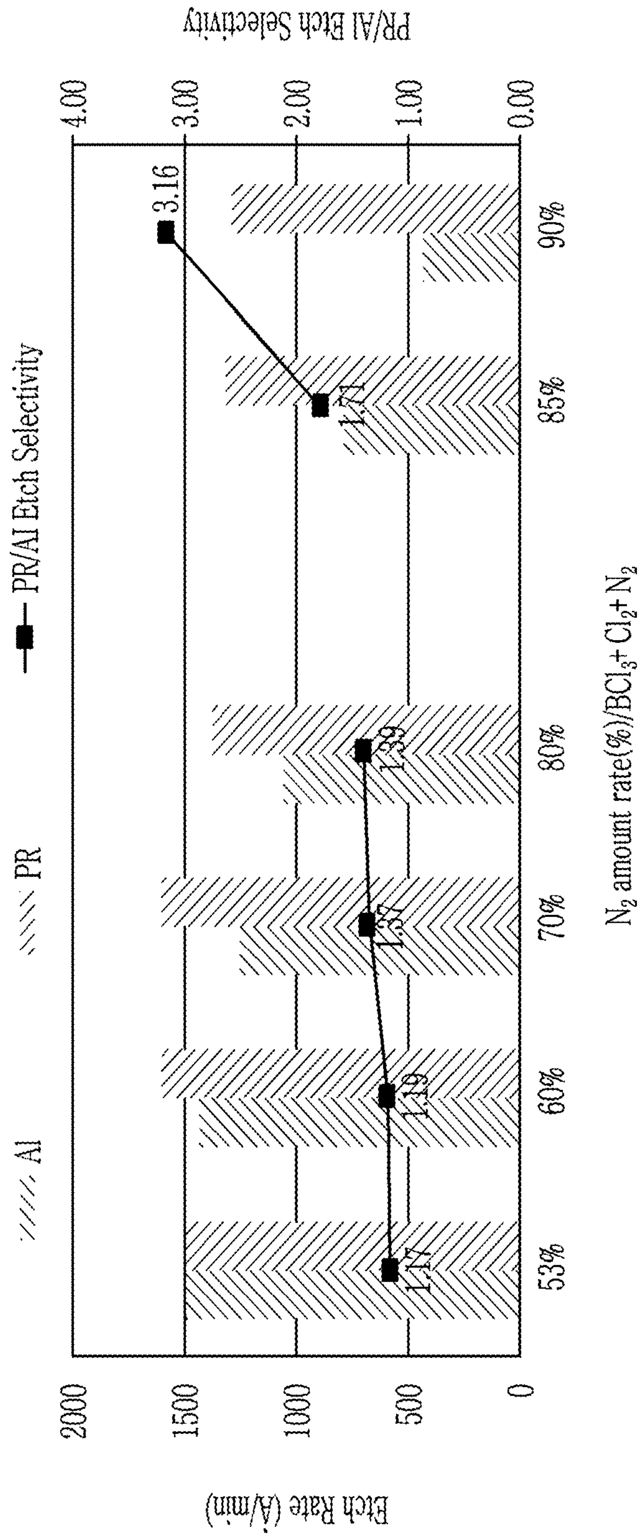


FIG. 9

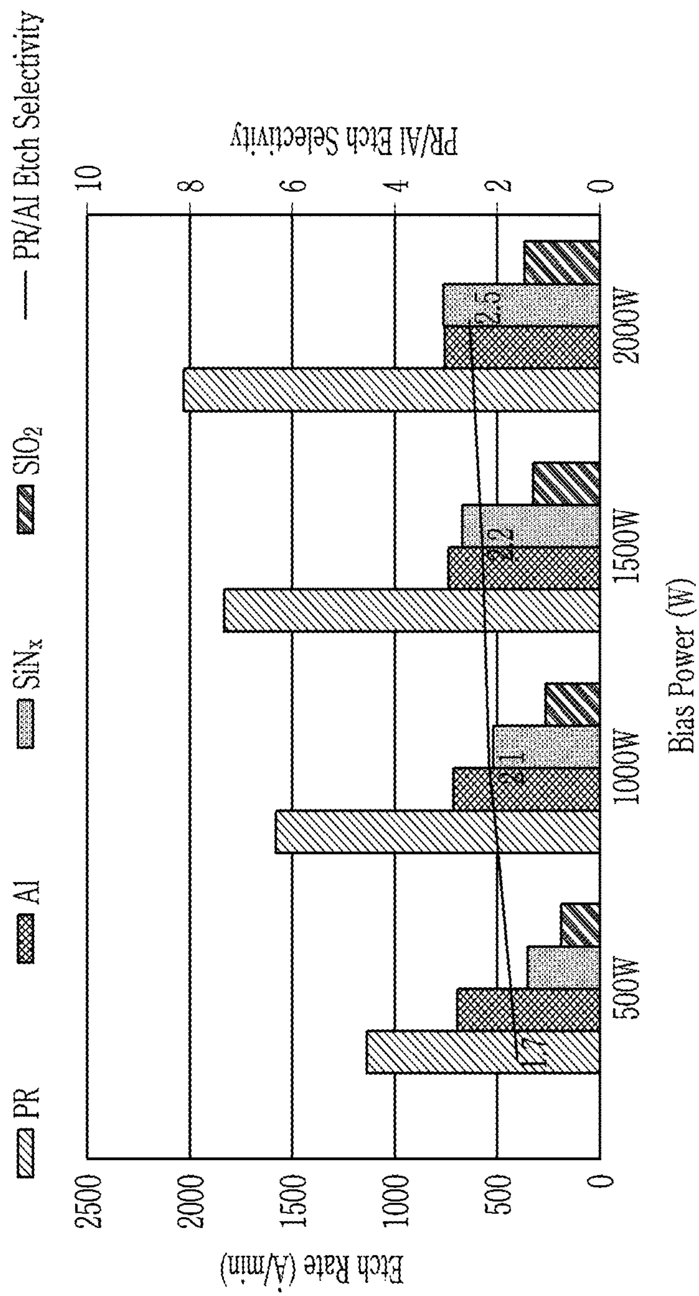


FIG. 10

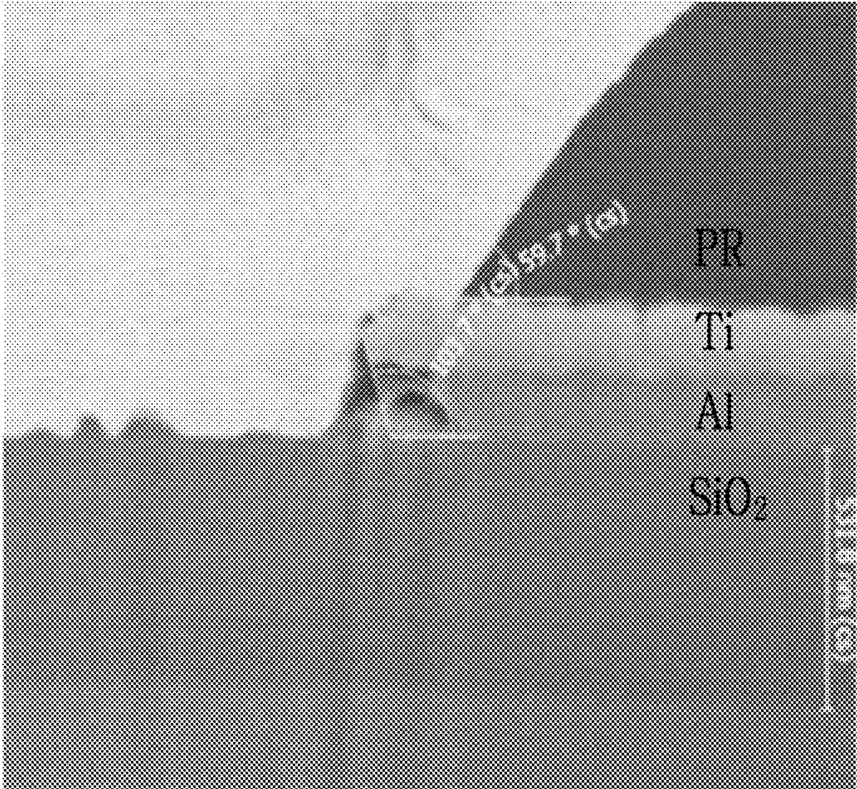


FIG. 11

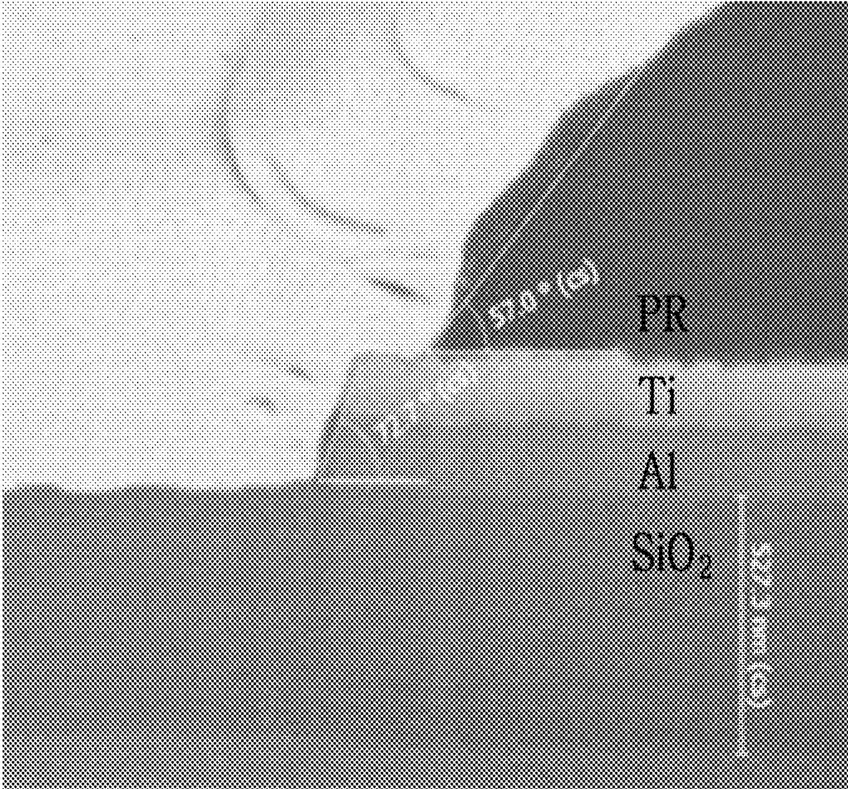


FIG. 12

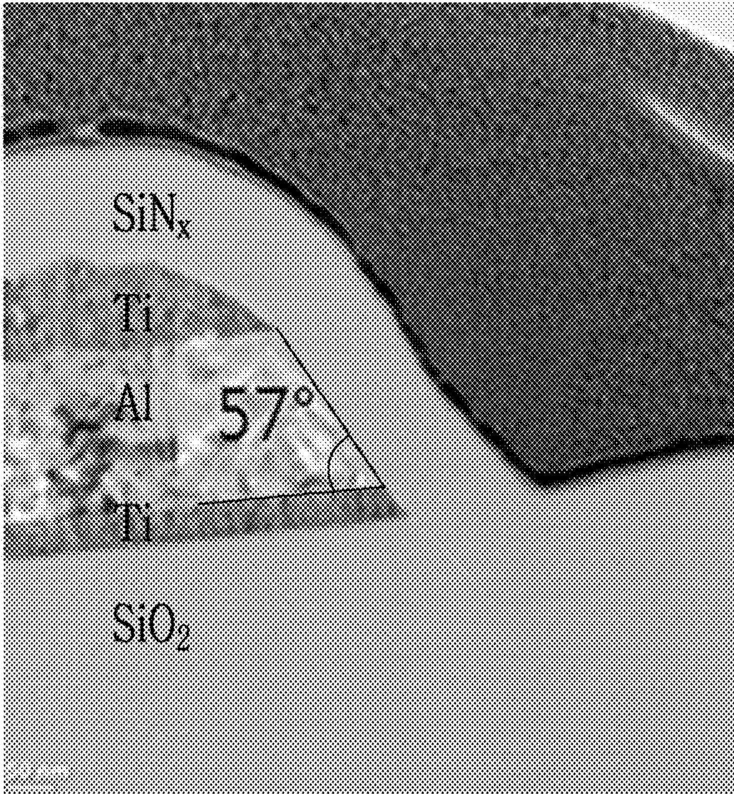
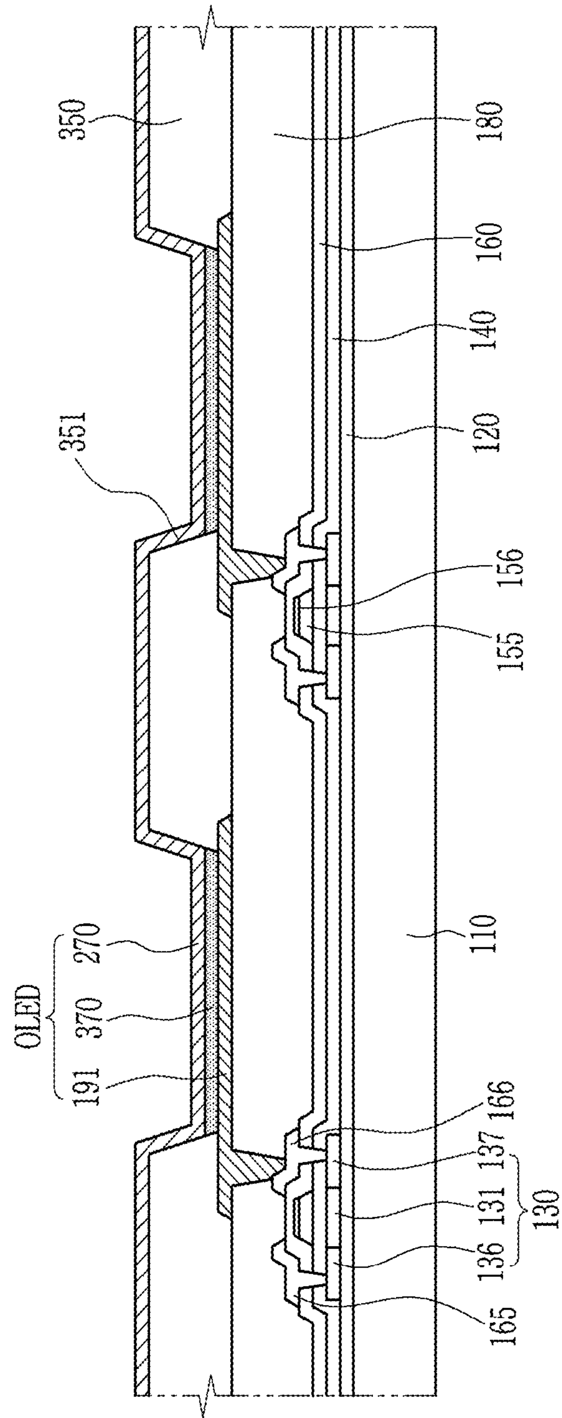


FIG. 13



ORGANIC LIGHT EMITTING DIODE DISPLAY AND MANUFACTURING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2018-0104793 filed in the Korean Intellectual Property Office on Sep. 3, 2018, the entire contents of which are incorporated herein by reference.

BACKGROUND

(a) Field

[0002] The present disclosure relates to an organic light emitting diode (OLED) display and a manufacturing method thereof.

(b) Description of the Related Art

[0003] An organic light emitting diode (OLED) of an organic light emitting diode (OLED) display includes two electrodes and an organic emission layer that is disposed between the two electrodes, and an electron injected from a cathode, which is one electrode, and holes injected from an anode, which is the other electrode, are combined in the organic emission layer to form an exciton, and the exciton emits light while emitting energy.

[0004] As the technology for the OLED display has been developed, the OLED display has become larger in size and higher in resolution. Accordingly, a problem such as a signal delay or a voltage drop may occur, and in order to solve the problem, the OLED display needs to be driven at a high speed.

[0005] The above information disclosed in this Background section is only for enhancement of understanding of the background of the inventive concept and therefore it may contain information that does not form the prior art that is already known in this country to a person of ordinary skill in the art.

SUMMARY

[0006] Exemplary embodiments of the present inventive concept provide an organic light emitting diode (OLED) display that can be prevented from being damaged during a manufacturing process, and implement high-resolution and high-speed driving, and a method for manufacturing the same.

[0007] An OLED display according to an exemplary embodiment includes: a substrate; a gate insulation layer that is disposed on the substrate; and a gate wire that is disposed on the gate insulation layer, and includes a gate electrode, wherein the gate wire includes a single layer of aluminum or an aluminum alloy, and an angle formed by side surfaces of the gate wire and the gate insulation layer is less than 65°.

[0008] The gate insulation layer may include a silicon oxide or a silicon nitride.

[0009] The OLED display may further include: a semiconductor layer that is disposed between the substrate and the gate insulation layer; and a source electrode and a drain electrode that are connected with the semiconductor layer, wherein the semiconductor layer may include a channel region, and the gate electrode overlaps the channel region.

[0010] The OLED display may further include: a pixel electrode that is connected to the drain electrode; an organic emission layer that is disposed on the pixel electrode; and a common electrode that is disposed on the organic emission layer.

[0011] A thickness of the gate wire may be less than 3000 Å.

[0012] The OLED display may further include a gate capping layer that is disposed on the gate wire, wherein the gate capping layer may include titanium (Ti) or a titanium nitride (TiNx).

[0013] Edges of an upper surface of the gate electrode and edges of a bottom surface of the gate capping layer may match.

[0014] An according to an exemplary embodiment, a method for manufacturing an OLED display is provided. The method includes: forming a gate insulation layer on a substrate; and forming a gate insulation layer on a substrate; and wherein the forming the gate wire includes: sequentially forming a conductive layer that includes aluminum or an aluminum alloy and a photoresist layer; forming a primary gate pattern by primarily dry etching the conductive layer; and forming a secondary gate pattern by secondarily dry etching the primary gate pattern, wherein the primary dry etching and the secondary dry etching use a mixed gas that contains chlorine (Cl_2) and nitrogen (N).

[0015] The mixed gas may further contain boron trichloride (BCl_3) or argon (Ar). A content of nitrogen (N) in the mixed gas during the primarily dry etching may be different from that during the secondary dry etching.

[0016] The content of nitrogen (N) in the mixed gas during the primarily dry etching is less than that during the secondary dry etching

[0017] In the primary dry etching, a content of nitrogen (N) in the mixed gas may be from about 10% to about 50%, and, in the secondary dry etching, a content of nitrogen (N) in the mixed gas may be from about 80% to about 90%.

[0018] A taper angle of the primary gate pattern may exceed 65°, and a taper angle of the secondary gate pattern may be less than 65°.

[0019] The gate insulation layer may contain a silicon oxide or a silicon nitride.

[0020] The forming the gate wire may further include forming an initial photoresist pattern by developing and exposing the photoresist layer, and a width of the initial photoresist pattern may match a width of a bottom surface of the gate wire.

[0021] A polymer layer that contains nitrogen (N) may be formed at side surfaces of each of the primary gate pattern and the secondary gate pattern.

[0022] A thickness of the gate wire may be less than 3000 Å.

[0023] The method for manufacturing the OLED display may further include forming a gate capping layer on the gate wire, wherein the gate capping layer may contain titanium (Ti) or a titanium nitride (TiNx).

[0024] A tertiary dry etching process is performed by using a gas that contains boron trichloride (BCl_3) or argon (Ar).

[0025] An etch selectivity of the photoresist layer to the aluminum or the aluminum alloy of the secondary dry etching may be greater than that of the primarily etching.

[0026] According to the exemplary embodiments, damage to the OLED display during a manufacturing process can be prevented, and high-resolution and high-speed driving of the OLED display can be enabled.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] FIG. **1** is a cross-sectional view of an organic light emitting diode display according to an exemplary embodiment of the present inventive concept.

[0028] FIG. **2** is a flowchart of a method for manufacturing an organic light emitting diode display according to an exemplary embodiment.

[0029] FIGS. **3**, **4**, **5**, **6** and **7** are cross-sectional views of each process of the manufacturing method of the organic light emitting diode display according to the exemplary embodiment.

[0030] FIG. **8** is a graph that shows etching selectivity of aluminum (Al) and the photoresist material PR depending on a content of nitrogen (N).

[0031] FIG. **9** is a graph that shows an etching ratio of each material depending on applied electrical power.

[0032] FIG. **10** is an image of a comparative example.

[0033] FIG. **11** is an image of an aluminum wire after primary dry-etching.

[0034] FIG. **12** is an image of an aluminum wire after secondary dry etching.

[0035] FIG. **13** is a cross-sectional view of an OLED display according to another exemplary embodiment.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0036] Hereinafter, the present inventive concept will be described more fully with reference to the accompanying drawings, in which exemplary embodiments of the inventive concept are shown. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present inventive concept.

[0037] The drawings and description are to be regarded as illustrative in nature and not restrictive. Like reference numerals designate like elements throughout the specification.

[0038] Further, since a size and a thickness of each element illustrated in the drawings are arbitrarily illustrated for convenience of description, the present inventive concept is not necessarily limited to those shown in the drawings. In the drawings, the thickness of layers, films, panels, regions, etc., are exaggerated for clarity. In addition, in the drawing, for convenience of description, the thickness of some of layers, films, panels, regions, etc., are exaggerated.

[0039] It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. The word "on" or "above" means positioned on or below the object portion, and does not necessarily mean positioned on the upper side of the object portion based on a gravitational direction.

[0040] In addition, unless explicitly described to the contrary, the word "comprise" and variations such as "comprises" or "comprising" will be understood to imply the inclusion of stated elements but not the exclusion of any other elements.

[0041] In addition, in this specification, the phrase "on a plane" means viewing a target portion from the top, and the phrase "on a cross-section" means viewing a cross-section formed by vertically cutting a target portion from the side.

[0042] Referring to FIG. **1**, an organic light emitting diode display according to an exemplary embodiment of the present inventive concept will be described. FIG. **1** is a cross-sectional view of an organic light emitting diode display according to an exemplary embodiment of the present inventive concept.

[0043] Referring to FIG. **1**, an organic light emitting diode display according to the present exemplary embodiment includes a substrate **110**. The substrate **110** may include a flexible material while is bendable, foldable, and rollable, such as plastic and the like. For example, the substrate **110** may include polyimide (PI), polyethylene naphthalate (PEN), polycarbonate (PC), polyarylate (PAR), polyether imide (PEI), polyether sulfone (PES), and the like.

[0044] A buffer layer **120** is disposed on the substrate **110**. The buffer layer **120** may include an inorganic material such as a silicon nitride (SiNx) and a silicon oxide (SiO_2). The buffer layer **120** is disposed between the substrate **110** and semiconductor layers **130**, which will be described later, and improves a quality of polysilicon by blocking an impurity from the substrate **110** during a crystallization process for forming the polysilicon and releases stress of the semiconductor layer **130** formed on the buffer layer **120** by planarizing the substrate **110**.

[0045] The semiconductor layers **130** are disposed on the buffer layer **120**. Each semiconductor layer **130** may be formed of polysilicon or an oxide semiconductor.

[0046] The semiconductor layer **130** may be formed of polysilicon, and includes a channel region **131**, a source region **136**, and a drain region **137**. The source region **136** and the drain region **137** are respectively disposed at opposite sides of the channel region **131**. The channel region **131** is an intrinsic semiconductor where an impurity is not doped, and the source region **136** and the drain region **137** are impurity semiconductors where a conductive impurity is doped. The semiconductor layer **130** may be formed of an oxide semiconductor, and in this case, an additional protective layer may be included to protect an oxide semiconductor material that is weak to an external environment such as a high temperature and the like.

[0047] A gate insulation layer **140** is disposed on the semiconductor layer **130** to cover the same. The gate insulation layer **140** may be a single layer or a multi-layer including at least one of a silicon nitride (SiNx) and a silicon oxide (SiO_2).

[0048] Gate electrodes **155** are disposed on the gate insulation layer **140**. Each gate electrode **155** is disposed to overlap the channel region **131** of the semiconductor layer **130**. The gate electrode **155** may have a trapezoidal shape of which a lower width is larger than an upper width in a cross-sectional view. A bottom surface of each gate electrode **155** may match an area that corresponds to the channel region **131** of each semiconductor layer **130**.

[0049] The gate electrode **155** is formed of a single layer of aluminum (Al) or an aluminum alloy. Aluminum (Al) has lower electrical resistance (Ω) than molybdenum (Mo). In the organic light emitting diode (OLED) display according

to the present exemplary embodiment, the gate electrode **155** includes a single layer of aluminum (Al) or an aluminum alloy, and thus resistance is low enough even through a thickness of the gate electrode **155** is thin, thereby transmitting a signal quickly. When the thickness is the same, the signal transmission speed of the gate electrode including a single layer of aluminum (Al) or an aluminum alloy is higher than that of the gate electrode including molybdenum (Mo), and thus the OLED display can be driven at a high speed.

[0050] The gate electrode **155** may have a thickness of less than 3000 Å. When the thickness of the gate electrode **155** is 3000 Å or exceeds 3000 Å, a pressure is locally applied to an area where the gate electrode **155** is disposed and thus a glass substrate attached for the post process may be damaged.

[0051] A taper angle of the gate electrode **155** is equal to 65° or less. The taper angle implies an angle formed by a side surface of the gate electrode **155** and the gate insulation layer **140**. When the taper angle of the gate electrode **155** exceeds 65°, an inorganic insulation layer formed above the gate electrode **155** may be disconnected or wirings formed above the gate electrode **155** and the gate electrode **155** may be short-circuited. However, in the organic light emitting diode display according to the present exemplary embodiment, the taper angle of the gate electrode **155** is equal to or less than 65°, and accordingly a defect, which may occur due to the taper angle of the gate electrode **155**, can be prevented.

[0052] The organic light emitting diode display according to the present exemplary embodiment includes a gate wire that transmits a gate signal and a data wire (not shown) that transmits a data signal. In FIG. **1**, the gate electrode **155** is illustrated as an example of the gate wire, but this is not restrictive. A feature of the above-stated gate electrode **155** can be applied at any portion in the gate wire that transmits the gate signal.

[0053] An interlayer insulation layer **160** is disposed on the gate electrode **155** and the gate insulation layer **140**. The interlayer insulation layer **160** may include a silicon nitride (SiNx) or a silicon oxide (SiO_2). Openings that respectively expose the source region **136** and the drain region **137** of the semiconductor layer **130** are respectively disposed in the gate insulation layer **140** and the interlayer insulation layer **160**.

[0054] A source electrode **165** and a drain electrode **166** are disposed on the interlayer insulation layer **160**. The source electrode **165** and the drain electrode **166** are respectively connected with the source region **136** and the drain region **137** of the semiconductor layer **130** through the openings that are respectively formed in the interlayer insulation layer **160** and the gate insulation layer **140**.

[0055] A passivation layer **180** is disposed on the interlayer insulation layer **160**, the source electrode **165**, and the drain electrode **166**. The passivation layer **180** planarizes steps formed by the interlayer insulation layer **160**, the source electrode **165**, and the drain electrode **166** by covering them, and thus a pixel electrode **191** can be formed on the passivation layer **180** without a step difference. The passivation layer **180** may be formed of an organic material such as a polyacrylate resin, a polyimide resin, or a stacked layer of an organic material and an inorganic material.

[0056] The pixel electrode **191** is disposed on the protective layer **180**. The pixel electrode **191** is connected with the drain electrode **166** through an opening formed in the passivation layer **180**.

[0057] A driving transistor formed of the gate electrode **155**, the semiconductor layer **130**, the source electrode **165**, and the drain electrode **166** is connected to the pixel electrode **191** and supplies a driving current to an organic light emitting diode (OLED). The organic light emitting diode display according to the present exemplary embodiment may further include a switching transistor (not shown) that is connected with a data line and transmits a data voltage in response to a scan signal, and a compensation transistor (not shown) that is connected with the driving transistor and compensates a threshold voltage of the driving transistor in response to the scan signal.

[0058] A partition wall **350** is disposed on the passivation layer **180** and the pixel electrode **191** to cover them, and the partition wall **350** includes a pixel opening **351** that exposes the pixel electrode **191**. The partition wall **350** may include an organic material such as a polyacrylate resin, a polyimide resin, and the like, or a silica-based inorganic material.

[0059] An organic emission layer **370** is disposed on a portion of the pixel electrode **191** that is exposed by the pixel opening **351**. The organic emission layer **370** may be formed of a low molecular weight organic material or a high molecular weight organic material such as PEDOT (poly(3, 4-ethylenedioxythiophene)). In addition, the organic emission layer **370** may be a multilayer including at least one of a functional layer such as a hole injection layer (HIL), a hole transport layer (HTL), an electron transport layer (ETL) and an electron injection layer (EIL).

[0060] The organic emission layer **370** may include a red organic emission layer, a green organic emission layer, and a blue organic emission layer. The red organic emission layer, the green organic emission layer, and the blue organic emission layer respectively emit red light, green light, and blue light such that a colored image can be realized.

[0061] A common electrode **270** is disposed on the organic emission layer **370**. The common electrode **270** may be disposed over a plurality of pixels. The pixel electrode **191**, the organic emission layer **370**, and the common electrode **270** may form the organic light emitting diode (OLED).

[0062] Here, the pixel electrode **191** may be an anode, which is a hole injection electrode, and the common electrode **270** may be a cathode, which is an electron injection electrode. However, the present exemplary embodiment is not limited thereto, and the pixel electrode **191** may be a cathode and the common electrode **270** may be an anode depending on a driving method of the organic light emitting diode display. The hole and electron are injected into the organic emission layer **370** from the pixel electrode **191** and the common electrode **270**, respectively, and an exciton generated by coupling the injected hole and electron falls from an excited state to a ground state to emit light.

[0063] An encapsulation layer (not shown) may be further disposed on the common electrode **270**. The encapsulation layer may include a plurality of layers, and may be formed as a complex layer including both an inorganic layer and an organic layer, or may be formed as a triple layer in which an inorganic layer, an organic layer, and an inorganic layer are sequentially stacked.

[0064] Hereinafter, a method for manufacturing an organic light emitting diode display according to an exemplary

embodiment will be described with reference to FIG. **2** to FIG. **7**. FIG. **2** is a flowchart of a method for manufacturing an organic light emitting diode display according to an exemplary embodiment.

[0065] Referring to FIG. **2**, a method for manufacturing an organic light emitting diode display according to an exemplary embodiment includes sequentially forming a conductive layer and a photoresist layer on a gate insulation layer (S**101**). The conductive layer is formed as a single layer of aluminum (Al) or an aluminum alloy. Next, a photoresist pattern is formed by exposing and developing the photoresist layer by using a photomask (S**102**). The photoresist layer may be formed as a positive or negative type of resist. Next, primary dry etching is carried out by using a mixed gas containing 10% to 50% of nitrogen (N) (S**103**). After the primary dry etching is carried out, secondary dry etching is carried out by using a mixed gas containing 80% to 90% of nitrogen (N) and applying a predetermined electrical power (S**104**). Through the two dry etching processes, a gate wiring pattern is formed. After the gate wiring pattern is formed, a residual photoresist pattern is removed (S**105**), and a subsequent process is carried out to complete an organic light emitting diode display.

[0066] FIG. **3** to FIG. **7** are cross-sectional views of each process of the manufacturing method of the organic light emitting diode display according to the exemplary embodiment.

[0067] Referring to FIG. **3**, a conductive layer **155-1** and a photoresist layer PRL, for example, a positive photoresist layer, are sequentially formed on a gate insulation layer **140**. The conductive layer **155-1** includes a single layer of aluminum (Al) or an aluminum alloy. When aluminum (Al) is included, resistance is low compared to a case in which molybdenum (Mo) is included. Thus, a wire formed of aluminum (Al) has a faster signal transmission speed than a wire formed of molybdenum (Mo) having the same thickness, and accordingly, the organic light emitting diode display can be driven at a high speed.

[0068] A photomask PM having a transmission portion T and a light blocking portion B on the photoresist layer PRL is disposed on the photoresist layer PRL, and light is applied to the photomask PM to expose and develop the photoresist layer PRL.

[0069] When the photoresist layer PRL is a positive-type resist, an exposed portion of the photoresist layer PRL is removed. In this case, the photomask PM has the blocking portion B in a portion that corresponds to a portion where a gate wire will be formed. On the other hand, when the photoresist layer PRL is provided as a negative-type resist, an exposed portion of the photoresist PRL remains. In this case, the photomask PM includes the transmission portion T in a portion that corresponds to a portion where a gate wire will be formed.

[0070] Referring to FIG. **4**, the photoresist layer PRL of FIG. **3** is exposed and developed such that a photoresist pattern PRP is formed. An area where the photoresist pattern PRP is disposed is an area that corresponds to the portion where the gate wire is formed. A width W of the photoresist pattern that is initially formed before an etching process is carried out may be the same as a width of the portion where the gate wire is formed.

[0071] Referring to FIG. **5**, primary dry etching is carried out on the conductive layer **155-1** of FIG. **4** such that a primary gate pattern **155-2** is formed. In the primary dry etching process, a mixed gas containing boron trichloride (BCl_3), chlorine (Cl_2), and nitrogen (N) is used. In the primary dry etching process, boron trichloride (BCl_3) may be replaced with argon (Ar).

[0072] An amount of nitrogen N in the mixed gas may be from about 10% to about 50%. The primary dry etching may be carried under a pressure of about 10 mTorr to 30 mTorr. Through the primary dry etching, a polymer layer that includes nitrogen (N) of the mixed gas and carbon (C) of the photoresist pattern PRP is formed at a side surface of the conductive layer **155-1**. Since the side surface of the conductive layer **155-1** is protected by the polymer layer, an undercut does not occur in the primary gate pattern **155-2** that includes aluminum (Al) or an aluminum alloy.

[0073] A width of a bottom side of the primary gate pattern **155-2** formed by the primary dry etching is larger than the width W of the initial photoresist pattern before the primary dry etching. The surface of the photoresist pattern PRP is also partially etched by the primary dry etching. Accordingly, the width of the photoresist pattern PRP becomes smaller than the width W of the initial photoresist pattern after the primary dry etching.

[0074] The shape of a cross-section of the primary gate pattern **155-2** may be trapezoidal of which a lower width is larger than an upper width. When a mixed gas that has a nitrogen (N) content of 10% to 50% is primarily used for dry-etching, an etching ratio of aluminum (Al) is larger than that of the photoresist material. That is, an etching rate of the conductive layer **155-1** that includes aluminum (Al) is higher than the retraction speed of the photoresist pattern PRP. In this case, the retraction speed represents an etching speed of the photoresist pattern PRP.

[0075] As a result, a taper angle A**1** formed by the side surface of the primary gate pattern **155-2** and the gate insulation layer **140** exceeds 65°, and thus the side surfaces of the primary gate pattern **155-2** become steep.

[0076] In the primary dry etching process, a dry etching process using a gas containing boron trichloride (BCl_3) and a dry etching process using a mixed gas containing chlorine (Cl_2) and nitrogen (N) may be individually carried out. In other words, the primary dry etching process may use a mixed gas containing chlorine (Cl_2) and nitrogen (N) and a tertiary dry etching process using a gas containing boron trichloride (BCl_3) may be carried out. In addition, in the tertiary dry etching process, boron trichloride (BCl_3) may be replaced with argon (Ar).

[0077] Referring to FIG. **6**, a secondary gate pattern **155-3** is formed by performing secondary dry etching on the primary gate pattern **155-2** of FIG. **5**. The secondary dry etching may be carried out through reactivity ion etching (RIE). A mixed gas used in the secondary dry etching contains boron trichloride (BCl_3), chlorine (Cl_2), and nitrogen (N). A content ratio of nitrogen (N) in the mixed gas may be from about 80% to about 90%. When the secondary dry etching is carried out, a predetermined electrical power may be applied. For example, an electrical power of 500 W to 2000 W may be applied. However, the intensity of the electrical power is not limited thereto, and may be less than 500 W or over 2000 W depending on the size of an object to be etched. In addition, the secondary dry etching may be carried out under a pressure of about 10 mTorr to 30 mTorr.

[0078] The shape of a cross-section of the secondary gate pattern **155-3** may be trapezoidal of which a lower width is larger than an upper width. When the secondary dry etching

is carried by using a mixed gas having a nitrogen content of 80% to 90% is carried by applying a predetermined electrical power, an etching ratio of the photoresist material is larger than that of aluminum (Al). That is, the retraction speed of the photoresist pattern PRP is higher than an etching rate of the primary gate pattern **155-2** that contains aluminum (Al). As a result, a taper angle A**2** formed by the side surface of the secondary gate pattern **155-3** and the gate insulation layer **140** is less than 65°, and thus the side surfaces of the secondary gate pattern **155-3** become not steep. Since a taper angle of a gate wire does not exceed 65°, a defect which may occur due to disconnection or short-circuit of an inorganic layer or a wire that is stacked in the next process may be prevented.

[0079] A width of a bottom side of the secondary gate pattern **155-3** formed by the secondary dry etching may be equal to the width W of the initial photoresist pattern. The surface of the photoresist pattern PRP is also partially etched by the secondary dry etching. Accordingly, the width of the photoresist pattern PRP after the secondary dry etching becomes smaller than the width of the photoresist pattern PRP after the primary dry etching.

[0080] Referring to FIG. **7**, a residual photoresist pattern PRP and a polymer layer formed at the side surfaces of the secondary gate pattern **155-3** may be removed by ashing. However, this is not restrictive, and any method that can remove the photoresist pattern PRP is applicable. Accordingly, a gate wire **155-4** having a taper angle of 65° or less is formed.

[0081] FIG. **8** is a graph that shows etching selectivity of aluminum (Al) and the photoresist material PR depending on a content of nitrogen (N). The content of nitrogen (N) implies a content ratio of nitrogen (N) in the mixed gas.

[0082] Referring to FIG. **8**, it can be observed that the PR/A**1** etch selectivity of the photoresist material PR to aluminum (Al) is increased as the content of nitrogen (N) in the mixed gas is increased. Thus, in the secondary dry etching process in which a content of nitrogen (N) is 80% to 90%, the photoresist pattern is etched faster than a gate pattern containing aluminum (Al). Accordingly, it is possible to form a small taper angle.

[0083] In a case that a gate wire of the organic light emitting diode display contains molybdenum (Mo), etch selectivity of the photoresist material and molybdenum (Mo) can be adjusted by using a mixed gas containing oxygen (O_2) in the etching process. However, when the gate wire includes aluminum (Al), aluminum (Al) reacts with oxygen (O_2) and thus AlO_x particles are generated, and accordingly oxygen (O_2) cannot be used. According to the exemplary embodiment of the present inventive concept, etch selectivity of the photoresist material and aluminum (Al) can be adjusted by etching using nitrogen (N_2) as an ambient gas.

[0084] FIG. **9** is a graph that shows an etching ratio of each material depending on an applied electrical power (bias power). Specifically, FIG. **9** shows an etch rate of each of the photoresist material PR, aluminum (Al), a silicon nitride (SiNx), and a silicon oxide (SiO_2), and PR/Al etch selectivity of the photoresist material PR to aluminum (Al) when a content of nitrogen (N) in the mixed gas is 85%.

[0085] Referring to FIG. **9**, the etch rate of the photoresist material PR and the etch selectivity of the photoresist material PR to aluminum (Al) are increased as the applied power is increased. Thus, in the secondary dry etching performed with nitrogen (N) content of 80% to 90% and a predetermined electrical power applied thereto, etching of the photoresist pattern PRP occurs faster than the primary gate pattern **155-2** that includes aluminum (Al). When the photoresist pattern PRP retracts rapidly, the upper surface of edge of the gate wire may be exposed to the mixed gas and side surfaces of the gate wire may be more smoothly formed, such that a taper angle formed by the side surfaces of the gate wire and the gate insulation layer may be formed to be small. In addition, a desired taper angle of the gate wire can be realized by adjusting the applied electrical power.

[0086] FIG. **10** is an image of a comparative example. FIG. **10** shows a cross-section of an aluminum wire that is formed on a silicon oxide (SiO_2) by performing dry-etching using a mixed gas of boron trichloride (BCl_3) and chlorine (Cl_2). Referring to FIG. **10**, when dry-etching is carried out by using a mixed gas which does not contain nitrogen (N), a bottom portion of the aluminum wire is excessively etched, thereby causing an under-cut.

[0087] FIG. **11** is an image of an aluminum wire after primary dry-etching. In FIG. **11**, an aluminum wire was formed on a silicon oxide (SiO_2) by performing dry-etching using a mixed gas that contained boron trichloride (BCl_3), chlorine (Cl_2), and nitrogen (N) with a content of 10% to 50%. In this case, unlike the comparative example of FIG. **10**, under-cut did not occur in a bottom portion of the aluminum wire. This is because a polymer layer that includes nitrogen (N) in the mixed gas and carbon (C) having a photoresist pattern is formed at side surfaces of the aluminum wire, thereby protecting the side surfaces of the aluminum wire.

[0088] Referring to FIG. **11**, a taper angle of the aluminum wire was as steep as 72.7°. This is because, as described above, when dry-etching is performed by using a mixed gas having nitrogen content of 10% to 50%, an etching rate of aluminum (Al) is larger than that of the photoresist material.

[0089] FIG. **12** is an image of an aluminum wire after secondary dry etching. In FIG. **12**, an aluminum wire is formed on a silicon oxide (SiO_2) by performing dry-etching using a mixed gas that contains boron trichloride (BCl_3), chlorine (Cl_2), and nitrogen (N) with a content of 80% to 90% and application of electrical power of 500 W to 200 W.

[0090] In FIG. **12**, a taper angle of the aluminum wire is 57°. Thus, compared to the comparative example of FIG. **11**, the taper angle of the aluminum wire was formed as small as less than 65°. This is because, when the dry-etching is performed by using a mixed gas having nitrogen content of 80% to 90% and applying a predetermined electrical power, an etching rate of aluminum (Al) is smaller than that of the photoresist material.

[0091] FIG. **13** is a cross-sectional view of an OLED display according to another exemplary embodiment. Description of the constituent elements that are the same as those in FIG. **1** will be omitted. Unlike the OLED display of FIG. **1**, the OLED display FIG. **13** further includes a gate capping layer **156** on a gate electrode **155**.

[0092] The gate electrode **155** includes aluminum (Al) or an aluminum alloy. The gate capping layer **156** includes titanium (Ti) or a titanium nitride (TiNx). The gate capping layer **156** can prevent the gate electrode **155** formed of aluminum (Al) from being damaged due to a buffered oxide etching (BOE) solution that is used in the next process.

[0093] Although the gate capping layer **156** is described as being disposed on the gate electrode **155**, it is not limited thereto. Referring to FIG. **12**, the gate capping layer **156**

may be disposed under the gate electrode **155**, or the gate capping layer **156** may be disposed on and under the gate electrode **155**.

[0094] The gate electrode **155** and the gate capping layer **156** of the OLED display according to the present exemplary embodiment may be formed by sequentially stacking a single layer of aluminum (Al) or an aluminum alloy and a layer that includes titanium (Ti) or a titanium nitride (TiNx), primarily dry-etching the two layers together, and then secondarily dry-etching the primarily dry-etched two electrodes. Accordingly, the gate electrode **155** and the gate capping layer **156** overlap each other, and edges of an upper surface of the gate electrode **155** and edges of a bottom surface of the gate capping layer **156** may match.

[0095] While this inventive concept has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood that the inventive concept is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is claimed is:

1. An organic light emitting diode (OLED) display comprising:

a substrate;

a gate insulation layer disposed on the substrate; and

a gate wire disposed on the gate insulation layer, the gate wire including a gate electrode,

wherein the gate wire comprises a single layer of aluminum or an aluminum alloy, and

an angle formed by side surfaces of the gate wire and the gate insulation layer is less than 65°.

2. The OLED display of claim **1**, wherein the gate insulation layer comprises a silicon oxide (SiO_2) or a silicon nitride (SiNx).

3. The OLED display of claim **2**, further comprising:

a semiconductor layer disposed between the substrate and the gate insulation layer; and

a source electrode and a drain electrode connected with the semiconductor layer,

wherein the semiconductor layer comprises a channel region, and

the gate electrode overlaps the channel region.

4. The OLED display of claim **3**, further comprising:

a pixel electrode connected to the drain electrode;

an organic emission layer disposed on the pixel electrode; and

a common electrode disposed on the organic emission layer.

5. The OLED display of claim **4**, wherein a thickness of the gate wire is less than 3000 Å.

6. The OLED display of claim **2**, further comprising a gate capping layer disposed on the gate wire,

wherein the gate capping layer comprises titanium (Ti) or a titanium nitride (TiNx).

7. The OLED display of claim **6**, wherein edges of an upper surface of the gate electrode and edges of a bottom surface of the gate capping layer match.

8. A method for manufacturing an organic light emitting diode (OLED) display, comprising:

forming a gate insulation layer on a substrate; and

forming a gate wire on the gate insulation layer,

wherein the forming the gate wire comprises:

sequentially forming a conductive layer that includes aluminum or an aluminum alloy and a photoresist layer;

forming a primary gate pattern by primarily dry etching the conductive layer; and

forming a secondary gate pattern by secondarily dry etching the primary gate pattern,

wherein the primary dry etching and the secondary dry etching use a mixed gas that contains chlorine (Cl_2) and nitrogen (N).

9. The method for manufacturing the OLED display of claim **8**, wherein the mixed gas further contains boron trichloride (BCl_3) or argon (Ar).

10. The method for manufacturing the OLED display of claim **8**, wherein a content of nitrogen (N) in the mixed gas during the primarily dry etching is different from that during the secondary dry etching.

11. The method for manufacturing the OLED display of claim **10** wherein the content of nitrogen (N) in the mixed gas during the primarily dry etching is less than that during the secondary dry etching.

12. The method for manufacturing the OLED display of claim **11**, wherein, in the primary dry etching, a content of nitrogen (N) in the mixed gas is from about 10% to about 50%, and

in the secondary dry etching, a content of nitrogen (N) in the mixed gas is 80% to 90%.

13. The method for manufacturing the OLED display of claim **12**, wherein

a taper angle of the primary gate pattern exceeds 65°, and

a taper angle of the secondary gate pattern is less than 65°.

14. The method for manufacturing the OLED display of claim **13**, wherein the gate insulation layer contains a silicon oxide (SiO_2) or a silicon nitride (SiNx).

15. The method for manufacturing the OLED display of claim **14**, wherein the forming the gate wire further comprises forming an initial photoresist pattern by developing and exposing the photoresist layer, and

a width of the initial photoresist pattern matches a width of a bottom surface of the gate wire.

16. The method for manufacturing the OLED display of claim **15**, wherein a polymer layer that contains nitrogen (N) is formed at side surfaces of each of the primary gate pattern and the secondary gate pattern.

17. The method for manufacturing the OLED display of claim **16**, wherein a thickness of the gate wire is less than 3000 Å.

18. The method for manufacturing the OLED display of claim **13**, further comprising forming a gate capping layer on the gate wire,

wherein the gate capping layer contains titanium (Ti) or a titanium nitride (TiNx).

19. The method for manufacturing the OLED display of claim **8**, further comprising a tertiary dry etching process performed by using a gas that contains boron trichloride (BCl_3) or argon (Ar).

20. The method for manufacturing the OLED display of claim **8**, wherein an etch selectivity of the photoresist layer to the aluminum or the aluminum alloy of the secondary dry etching is greater than that of the primarily etching.

* * * * *

patsnap

专利名称(译)	有机发光二极管显示器及其制造方法		
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[标]申请(专利权)人(译)	三星显示有限公司		
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摘要(译)

根据示例性实施方式的OLED显示器包括：基板； 栅极绝缘层，其设置在基板上； 以及设置在栅极绝缘层上并包括栅电极的栅极线，其中，栅极线包括铝或铝合金的单层，以及由栅极线和栅极绝缘层的侧面形成的角度 小于65°。